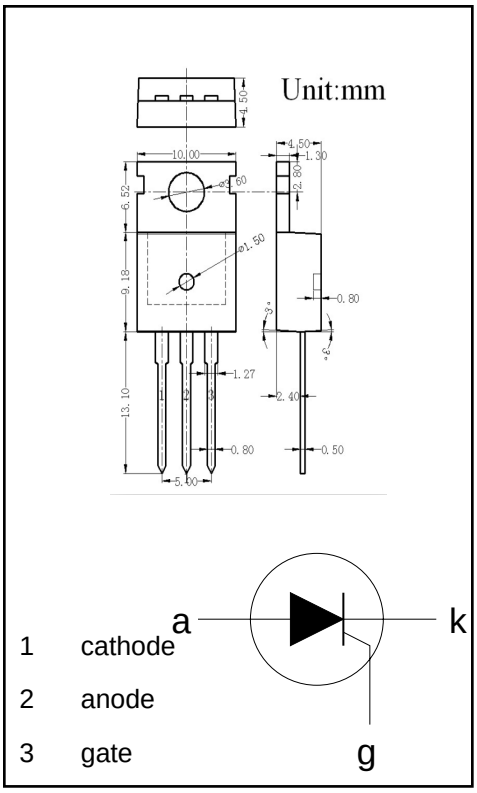
SHENZHEN LONG JING MICRO-ELECTRONICS CO., LTD.

TO-220 **Plastic-Encapsulate MOSFETS**

BT152-800R



GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectionalblockingvoltage capabilityandhighthermalcycling performance.Typicalapplications includemotorcontrol,industrialand domesticlighting,heatingandstatic switching.

QUICK REFERENCE DATA

SYMBO	LPARAMETER			MAX.	UNIT
		BT152-		**800R**	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages			800	V
$I_{T(AV)}$	Average on-state current			13	A
$I_{T(RMS)}$	RMS on-state current			20	A
I_{TSM}	Non-repetitive peak on-state			200	A

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
				-800R	
V_{DRM}	Repetitive peak off-state-voltages			800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 103$ ˚C	-	13	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	20	A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; T_j = 25 ˚C prior to surge			
		t = 10 ms	-	200	A
		t = 8.3 ms	-	220	A
I^2t	I^2t for fusing	t = 10 ms	-	200	A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 50 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs	-	200	A/µs
I_{GM}	Peak gate current		-	5	A
V_{GM}	Peak gate voltage		-	5	V
V_{RGM}	Peak reverse gate voltage		-	5	V
P_{GM}	Peak gate power		-	20	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5	W
T_{stg}	Storage temperature		-40	150	˚C
T_j	Operating junction temperature		-	125	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	3	32	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	25	80	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	15	60	mA
V_T	On-state voltage	I_T = 40 A	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.2	1.0	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform gate open circuit	200	300	-	V/µs
t_{gt}	Gate controlled turn-on time	$V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs; I_{TM} = 40 A	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 50 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

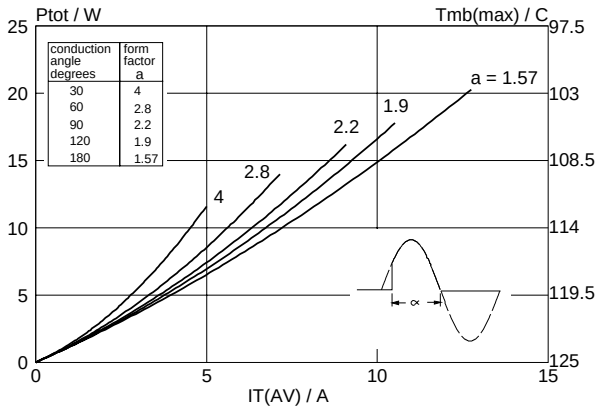


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

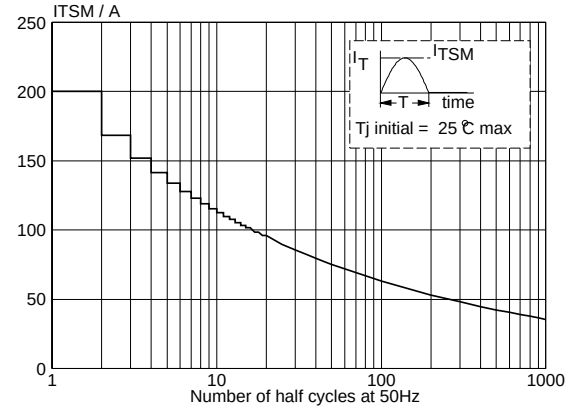


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

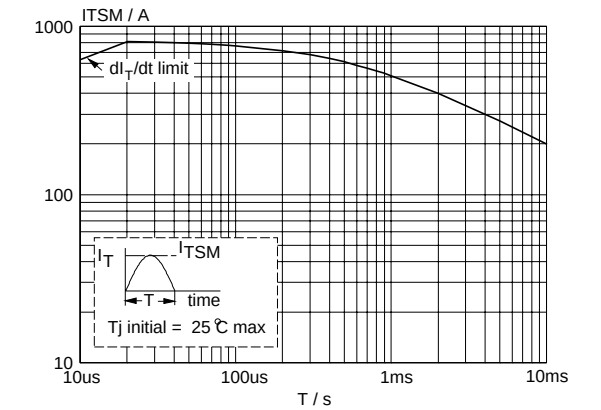


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 10$ms.

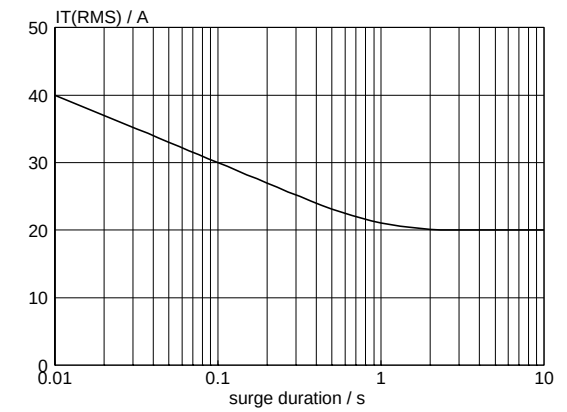


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 103$˚C.

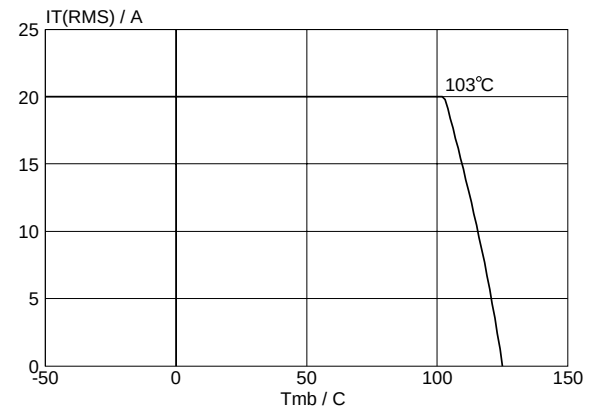


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

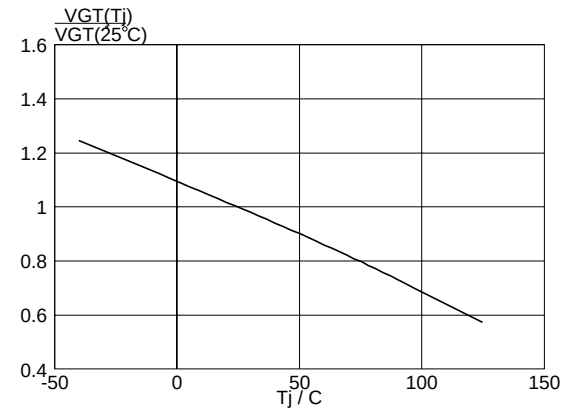


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ $V_{GT}(25˚C)$, versus junction temperature T_j.

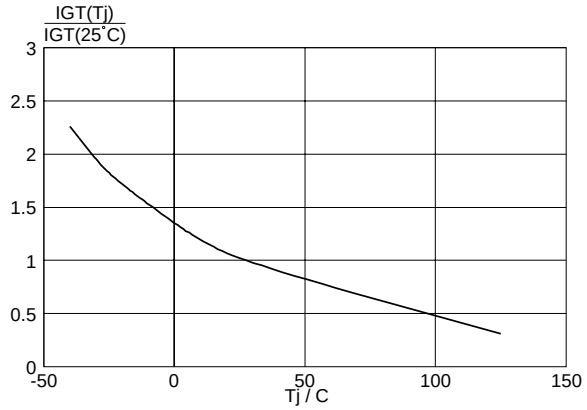


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

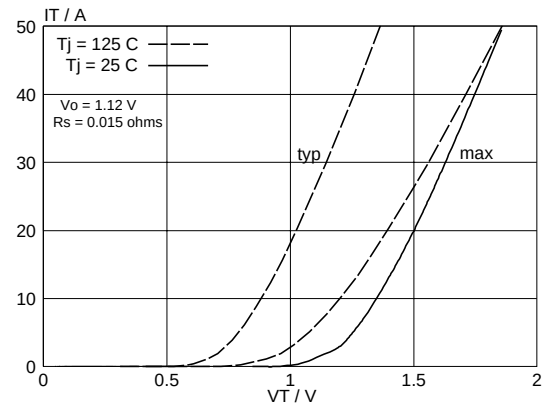


Fig.10. Typical and maximum on-state characteristic.

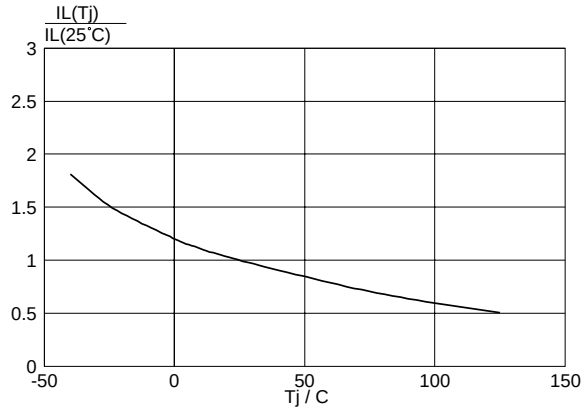


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

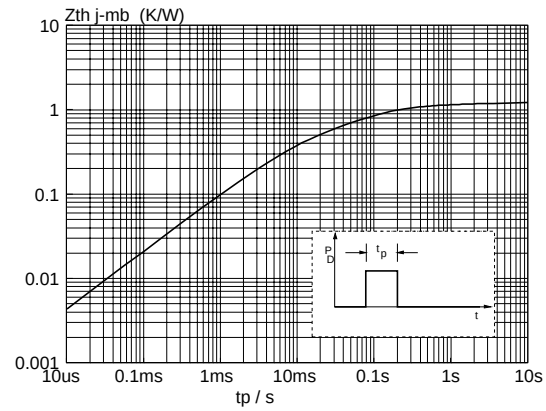


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

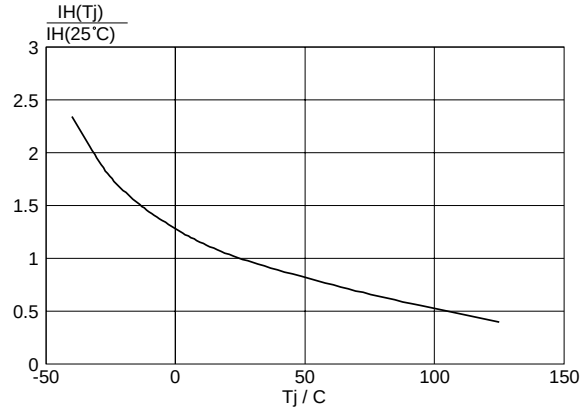


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

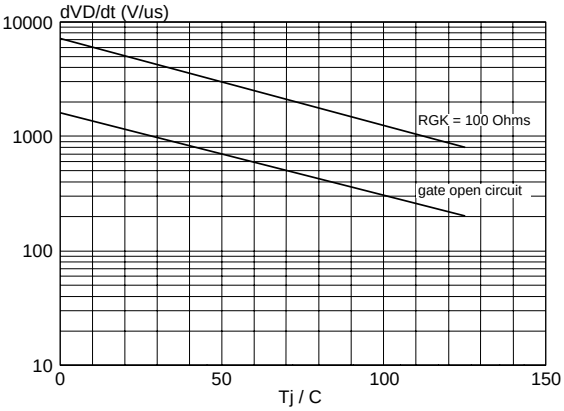


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.